REMARKS

In response to the Official Action mailed on September 28, 2007, the Applicants request reconsideration of the rejections of the claims based on the following remarks.

A typographical error was noted in claims 8 and 11. Specifically, "completely cured" was mistyped as "completed cured" in both claims. The Applicants propose to amend these two claims to correct these errors. The proposed amendments do not affect the scope of the claims.

Examiner Singal and Examiner Matthew Smith are thanked for their courtesy in granting an interview to discuss the present application on October 9, 2007. The specific issues discussed at the interview are described below in connection with the rejections and objections.

On page 2 of the Official Action, the drawings were objected to under 37 CFR 1.83(a). In the interview held on October 9, 2007, the objection to the drawings was withdrawn.

On page 3 of the Official Action, claims 8 and 10 - 13 were rejected under 35 USC 102(b) as anticipated by Segawa et al (JP 2002-026070, referred to below as Segawa). This rejection is respectfully traversed.

As discussed at the interview, the inventions described by independent claims 8 and 11 are fundamentally different from the method disclosed by Segawa in that during the process described in claims 8 and 11 of heating a resin composition disposed between opposing terminals (claim 8) or between opposing electrode pads and circuit electrodes (claim 11), the opposing terminals or the opposing electrode pads and circuit electrodes are separated from each other by a space large enough to enable the particles to move laterally inside the space, whereby the particles can collect between the opposing terminals or the opposing electrode pads and circuit electrodes by melting and agglomeration of the electrically conductive particles. It is impossible for such a state to occur in the method disclosed in Segawa.

To assist the Examiner in better understanding Segawa, a verified translation of Segawa has been prepared and is submitted as Attachment A of this amendment. As can be seen from this translation, Segawa discloses a method of manufacturing a semiconductor device in which an IC chip is joined to a wiring board by an anisotropic electrically conductive material containing meltable electrically conductive particles. Segawa discloses a first embodiment in Figure 1 in which a bare chip IC 4 having bumps 3a, 3b formed on connecting electrodes 4a, 4b, etc. is connected to the electrodes 2a, 2b, etc. of a wiring board 1 by an anisotropic electrically conductive material 7 containing meltable electrically conductive particles 6a, 6b,

etc. Figure 6 shows a second embodiment in which connecting electrodes 24a, 24, etc. of a bare chip IC 24 are connected to the electrodes 22a, 22b, etc. of a wiring board 21 by an anisotropic electrically conductive material 27 containing meltable electrically conductive particles 26a, 26b, etc. without use of bumps.

The process used to form the embodiment of Figure 1 is illustrated in Figure 3 and described in paragraphs 0038 - 0044 of Segawa. As described in these paragraphs, an anisotropic electrically conductive material 7 in the form of a sheet or a paste is first applied atop the electrodes 2a, 2b, 2c ... 2n of a wiring board 1 (paragraphs 0040 - 0041).

Next, a bare chip IC 4 having solder bumps 3a, 3b formed atop connecting electrodes 4a, 4b, 4c ... 4n is sucked by a bonding tool 14, and the solder bumps 3a, 3b are aligned with the electrodes 2a, 2b, 2c . . . 2n of the wiring board 1 (paragraph 0042).

Next, a bonding tool 14 having a heating function is used in order to apply heat and pressure to the bare chip IC 4 to bond the electrodes 2a, 2b, 2c ... 2n of the wiring board 1 and the solder bumps 3a and 3b to each other (paragraph 0043).

Finally, the insulating resin 5 of the anisotropic electrically conductive material 7 is thermally set (paragraph

0044).

The process used to form the embodiment of Figure 6 of Segawa is illustrated in Figure 7 and described in paragraphs 0060 - 0067. As described in these paragraphs, first, an anisotropic electrically conductive material 27 in the form of a sheet or a paste is applied atop the electrodes 22a, 22b, 22c ... 22n of a wiring board 21 (paragraph 0063).

Next, a bare chip IC 24 is sucked by a bonding tool 34 and is placed atop the electrically conductive material 27 with the connecting electrodes 24a, 24b, 24c ... 24n of the bare chip IC 24 aligned with electrodes 22a, 22b, 22c ... 22n of the wiring board 21 (paragraph 0064).

Next, using a bonding tool having a heating function, the electrically conductive particles 26a, 26b, 26c ... 26n in the anisotropic electrically conductive material 27 are melted by heating to electrically connect the electrodes 22a, 22b, 22c ... 22n of the wiring board 21 to the connecting electrodes 24a, 24b, 24c ... 24n of the bare chip IC 24 (paragraph 0066).

Finally, the insulating resin 25 of the anisotropic electrically conductive material 27 is heated and cured (paragraph 0067).

In both embodiments, during the step of heating the

anisotropic electrically conductive material 7, 27 in order to melt the electrically conductive particles 6, 26, the bare chip IC 4, 24 is pressed against the wiring board 1, 21 so as to restrain the electrically conductive particles 6, 26 present between the connecting electrodes of the bare chip IC 4, 24 and the electrodes of the wiring board 1, 21 against any lateral movement. This fact is clear with respect to the embodiment of Figure 1 from paragraph 0043 which specifically mentions the application of heat and pressure. It is also clear from the first sentence of paragraph 0050, which states that

> This method has the merit that the bare chip IC 4 is pressed at the time of solder bonding and electrical connection can be realized with certainty ...

The description of the embodiment of Figure 6 does not mention the application of pressure during heating, but the application of pressure to the bare chip IC 24 is inherent in the use of the same type of bonding tool to bond the bare chip IC 24 to the wiring board 21 as is used in the embodiment of Figure 1 (paragraph 0061). Both Figure 6 and Figure 7(e) clearly show a single layer of particles 26a, 26b, etc. sandwiched and restrained between the connecting electrodes 24a, 24b, etc. of a bare chip IC 24 and the electrodes 22a, 22b, etc. of a wiring board 21.

As such, it is clear that neither embodiment of Segawa includes a step of heating in which opposing terminals (as in

claim 8) or opposing electrode pads and circuit electrodes (as in claim 11) are separated from each other by a space large enough to enable particles to move laterally inside the space to enable the particles to collect between the opposing terminals or opposing electrode pads and circuit electrodes by melting and agglomeration of the electrically conductive particles as set forth in claims 8 and 11.

Segawa does not disclose the magnitude of the pressure which is applied to a bare chip IC 4, 24 by a bonding tool 14, 34 when bonding the bare chip IC to a wiring board 1, 21. However, the basic parameters of the mounting technique employed in Segawa were well known to those skilled in the art well before the Segawa reference, and in this well known mounting technique, it was the standard procedure for an IC chip to be pressed against a wiring board with a pressure so as to immobilize the electrically conductive particles in an anisotropic electrically conductive medium between the opposing electrodes of an IC chip and a wiring board.

Prior art references illustrating this fact are plentiful. One example of such a reference is JP 11-4064 A1 (1999), which is of record in the present application and which discloses a mounting method using an anisotropic electrically conductive paste. Paragraphs [0010] - [0012] of that reference describe the mounting method in detail:

[0010] Figure 2 is a cross-sectional view showing a step of mounting an LSI on a mounting substrate using the anisotropic electrically conductive resin shown in Figure 1. Here, a FC (flip chip)-type LSI is used as the LSI 10. First, as shown in Figure 2(a), in the state before the LSI 10 is mounted on a mounting substrate 20, the anisotropic electrically conductive resin 1 of Figure 1 is thinly applied atop the electrode pads 21 of the mounting substrate 20. In this state, the solder particles 3 in the resin 2 are not contacting each other and are in their original state. Metal bumps 12 are formed on the surface of the electrode pads 11 of the LSI 10 being mounted. As is well known, the metal bumps 12 can be easily formed to a small size by a metal plating method.

[0011] Next, as shown in Figure 2(b), in a state in which the electrode pads 11 or the metal bumps 12 of the LSI 10 and the electrode pads 21 on the mounting substrate 20 are superposed in alignment with each other, **the LSI 10 is pressed towards the mounting substrate 20**. As a result, in the region immediately beneath the metal bumps 12 of the LSI 10, **the anisotropic electrically conductive resin 1 is compressed, so the solder particles 3 contained in this region are made to contact each other, and a state is achieved in which the metal bumps 12 and the electrode pads 21 are electrically contacting**. In contrast, in regions other than the metal bumps 12, the anisotropic electrically conductive resin 1 is not compressed, or the compressive force is low, so the solder particles 3 are in their original state, and electrical contact is not obtained. However, the electrical connection which is obtained at this time between the metal bumps 12 and the electrode pads 21 is obtained by contact between the solder particles 3, so the electrical resistance is relatively high.

[0012] Next, as shown in Figure 2(c), in a state in which the compression between the LSI 10 and the mounting substrate 20 is maintained, heat is applied to

the entire body, and the resin 2 of the anisotropic electrically conductive resin 1 is thermally set. At the same time, the solder particles in the anisotropic electrically conductive resin 1 are melted, and the metal bumps 12 and the electrode pads 21 are soldered by the molten solder 3'. Heating is then stopped, the molten solder 3' is solidified, the metal bumps 12 and the electrode pads 21 are firmly soldered in a state with low electrical resistance, and the resin 2 in the anisotropic electrically conductive resin 1 is cured to maintain the spacing between the LSI 10 and the mounting substrate 20, and the LSI 10 and the mounting substrate 20 are adhered by the adhesive force of the resin 2. As a result, an LSI and a mounting substrate can be electrically connected with a low resistance equal to that of usual soldering and in a more stable condition than by soldering, and the method can be applied to mounting of high performance LSI's demanding a decreased resistance of connection portions to mounting substrates.

Another example is the book "CSP/MCM Mounting Technology", published in 1999, which discloses a similar mounting method using an adhesive layer containing conductive particles to join an IC chip to a wiring board. A copy of pages 182 - 185 of this book is attached to this amendment as Attachment B. Page 182 describes what it calls the "flip tack method" in which an adhesive has a two-layer structure comprising an upper layer of an adhesive and a lower layer of an adhesive having electrically conductive particles dispersed in it. According to the description on page 182,

In connection by flip tack, as shown by Figure 1, the electrically conductive particle layer-side is

placed atop a substrate such as a printed wiring board (PWB) or a flexible wiring board (FPC), a chip and the substrate are aligned, and heating is performed at 170 - 190°C for 10 - 20 seconds **in a state in which a pressure of 50 - 150 MPa is applied** from the chip side (a prescribed pressure is selected based on the total surface area of bumps) to connect the chip and the substrate. The space between the chip and the substrate is filled by melting and flow of the adhesive in the heating and pressing step. **The electrically conductive particles are captured between the electrodes**, and the bumps of the chip and the electrodes of the substrate **are electrically connected by the captured electrically conductive particles.**

Pages 184 and 185 of this reference describe an electron microscope photograph of a cross section of the bond between an IC chip and a printed wiring board formed by the "flip tack method". The bottom paragraph on page 184 reads as follows:

Figure 7 is a photograph of a cross section of a joint portion. From this photograph, it can be seen that electrically conductive Ni particles **have become embedded** in the Au bumps of the chip and the substrate electrodes. This embedding is thought to contribute to the high reliability exhibited by Figures 4 - 6.

The pressure of 50 - 150 MPa applied to solder bumps in this reference corresponds to 7250 to 21750 psi.

Yet another reference is "ThreeBond Technical News" (July, 1996) (Attachment C), which describes the use of various anisotropic electrically conductive adhesives sold by ThreeBond

Corporation of Tokyo, Japan to form electrical connections. According to page 2 of this document,

> An anisotropic electrically conductive adhesive performs electrical connection of opposing electrodes and secures them in a single step. It can be used for materials which cannot be joined by soldering or which cannot withstand the high temperatures of soldering.
>
> The material of an anisotropic electrically conductive adhesive is constituted by an adhesive (binder) for securing electrodes to each other and electrically conductive particles which are uniformly dispersed in the binder. The binder components must of course have adhesive strength, they must maintain electrical resistance such that adjoining electrodes do not conduct, and they must be reliable materials ....
>
> As shown in Figure 1, the electrically conductive particles are disposed between electrodes. Accordingly, they must stably provide electrical conduction between opposing electrodes, and they must have a shape and dispersed number so that there is no conduction between adjoining electrodes ....
>
> In bonding operation, essentially, **a binder is pressed and spread by heat and pressure, and electrically conductive particles are made to contact electrodes.** There are also cases in which a binder which is cured by ultraviolet light or the like instead of heat is used.

Table 4 on page 5 of this document gives the following suggested conditions for compressive bonding using ThreeBond 3773, which is a printable anisotropic electrically conductive adhesive in the form of a paste used for connecting electrodes of

small liquid crystal panel displays:

Table 4

Suggested connecting conditions for ThreeBond 3373

Pressure bonding temperature (°C)	120 - 160
Applied pressure (MPa) (kgf/cm^2)	2.9 (30)
Length of pressure bonding (sec)	5 - 10

The pressure of 30 kgf/cm^2 given in Table 4 corresponds to 426.7 psi.

From the above-described three references, it can be seen that well before the Segawa reference, methods of bonding an IC to a substrate using an anisotropic electrically conductive material were both well known and commercially practiced. In these conventional methods, it was customary to press an IC chip against a substrate with sufficiently high pressure to immobilize electrically conductive particles in the anisotropic electrically conductive medium between the electrodes of the IC chip and the electrodes of the substrate and even to embed the particles in the electrodes of the substrate, as described above in "CSP/MCM Mounting Technology".

The only difference between Segawa and pre-existing mounting methods using an anisotropic electrically conductive material appears to be that in the Segawa reference, the resin in the

anisotropic electrically conductive material has a curing rate of 0% at the melting point T2 of the electrically conductive particles (see paragraph 047), while the references mentioned above do not specify the curing rate of a resin at the time of melting of electrically conductive particles dispersed in the resin. The basic steps in the method, i.e., applying an anisotropic electrically conductive material to a substrate, disposing an IC chip atop the anisotropic electrically conductive material, applying heat and pressure to the IC chip to produce intimate contact by electrically conductive particles in the anisotropic electrically conductive material with opposing electrodes of the IC chip and the substrate, and then curing the resin in the anisotropic electrically conductive material, are the same in the Segawa reference and in the conventional methods. Even though Segawa does not specify the pressure which is applied to an IC chip 4, 24 by a bonding tool 14, 34 during bonding, in light of the fact that Segawa is basically the same as existing methods of bonding using an anisotropic electrically conductive material, a person skilled in the art would have known from the teachings of the prior art that the pressure applied by the bonding tool 14, 34 in Segawa should be of a level to immobilize the electrically conductive particles 6, 26 in the anisotropic electrically conductive material 5, 25 between opposing electrodes of an IC chip 4, 24 and a wiring board 1, 21.

As such, it is clear to a person skilled in the art that the method disclosed by Segawa does not include a step of heating a

resin composition disposed between opposing terminals (as in claim 8) or between opposing electrode pads and circuit electrodes (as in claim 11) with the opposing terminals or the opposing electrode pads and circuit electrodes separated from each other by a space large enough to enable the particles to move inside the space with the electrically conductive particles collecting between the opposing terminals or between the opposing electrode pads and circuit electrodes by melting and agglomeration of the electrically conductive particles, as set forth in independent claims 8 and 11.

Accordingly, as Segawa does not disclose all the features of independent claims 8 or 11, it cannot anticipate these claims or dependent claims 10, 12, and 13 which depend therefrom. All of claims 8 and 10 - 13 are therefore allowable.

The invention described by claims 8 and 11 results in a totally different structure from that obtained by the method employed in Segawa. In Segawa, there is no agglomeration of particles in the spaces between opposing electrodes which are being interconnected, and instead the electrodes are electrically connected with each other by isolated electrically conductive particles sandwiched between the electrodes. This results in the electrical connections having a high electrical resistance and also limits the height of the joints between the electrodes to at most the diameter of the electrically conductive particles.

In contrast, on account of the agglomeration of particles which occurs in the invention described by claims 8 and 11, it is possible to obtain a joint having a large height and a large surface area of contact with the terminals or electrodes, thereby achieving an electrical connection of low resistance.

Claim 13 further patentably distinguishes the present invention from Segawa. Claim 13, which depends from claims 11 and 12, states that substantially all of the electrically conductive particles in a resin composition, which completely fills the space between a semiconductor chip and a circuit substrate, collect in regions between opposing electrode pads and circuit electrodes. The "regions between opposing electrode pads and circuit electrodes" in claim 13 refer to the plurality of regions each of which is disposed between one of the electrodes pads on a semiconductor chip and the opposing circuit electrode on a circuit substrate. There are as many of these regions as there are opposing pairs of electrode pads and circuit electrodes. A point situated between two adjoining electrode pads or circuit electrodes, or example, does not lie within any these regions, since such a point is not disposed between an electrode pad and the opposing circuit electrode.

In rejecting this claim, page 6 of the Official Action relied upon Figure 7(e) of Segawa. However, from even a cursory view of this figure, it can be seen that this figure does not illustrate a situation in which substantially all the

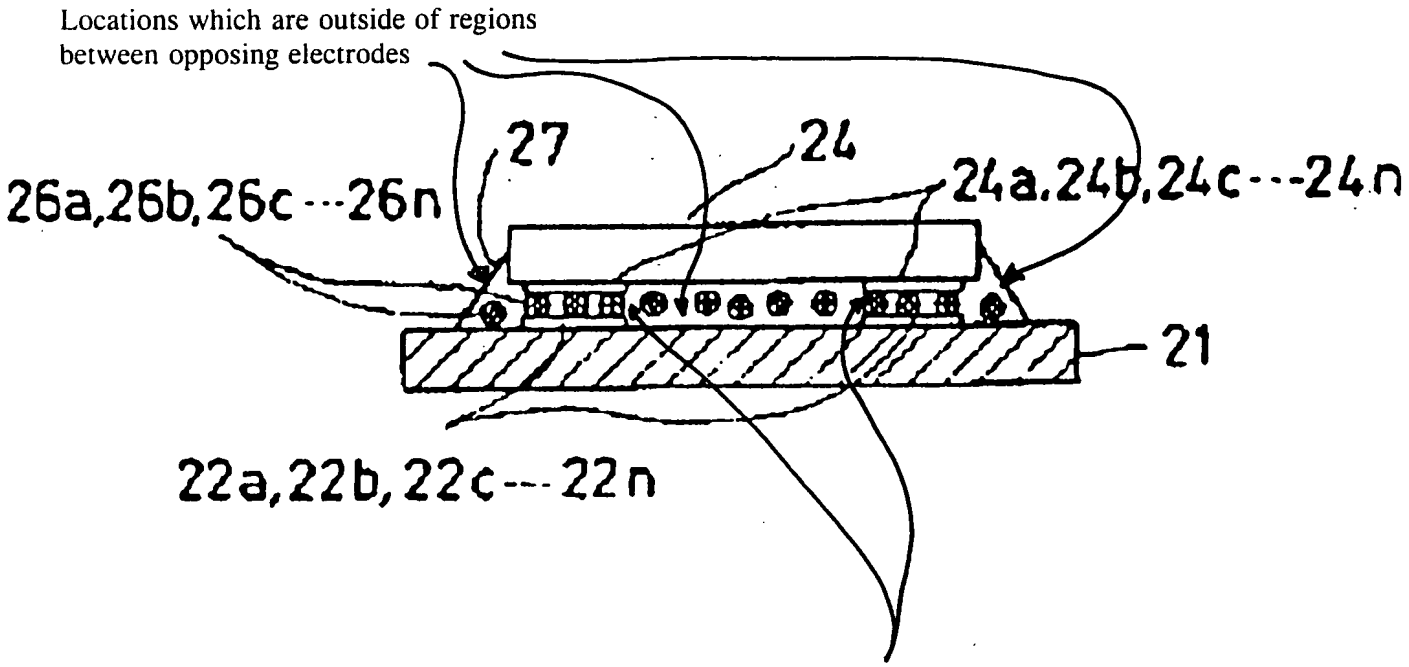
electrically conductive particles 26a, 26b, etc. in the anisotropic electrically conductive material 27 of Figure 7(e) have collected in the regions between opposing electrode pads and circuit electrodes, for there are more electrically conductive particles 26a, 26b, etc. outside the regions between opposing electrodes than there are electrically conductive particles inside the regions between opposing electrodes. Figure 7(e) shows six electrically conductive particles (not numbered in the figure) trapped in two regions between opposing connecting electrodes 24a, 24b, etc. of an IC chip 24 and the electrodes 22a, 22b, etc. of a wiring board 21, while the remaining seven electrically conductive particles in the anisotropic electrically conductive material 27 are located outside of the regions between opposing electrodes. Even though Figure 7(e) of Segawa is but a schematic representation, it clearly shows the fact that in the method of Segawa, electrically conductive particles do not collect in the spaces between opposing electrodes so that substantially all of the electrically conductive particles in a resin composition have collected in regions between opposing electrode pads and circuit electrodes as set forth in claim 13. As such, claim 13 does not read on Figure 7(e) of Segawa, so Segawa cannot anticipate this claim.

An example of arrangement on which claim 13 does in fact read is the embodiment shown in Figures 12(a) and 12(b) of the present application. As described on pages 30 and 31 of the specification of the present application, Figure 12(a) shows a

state prior to heating in which the entire space sandwiched between a semiconductor chip 20 and a substrate 10 is filled with an electrically conductive adhesive 1b comprising a resin 2b and electrically conductive particles 3b. At this time, the electrically conductive particles 3b are dispersed substantially uniformly throughout the entire space. Figure 12(b) shows the state after the assembly of Figure 12(a) has been heated to a temperature higher than the melting point of the electrically conductive particles 3b to enable the electrically conductive particles 3b to collect by melting and agglomeration. In this state, all of the electrically conductive particles 3b have collected by melting and agglomeration on the surfaces of the opposing electrode pads 21 of the semiconductor chip 20 and the lands 11 of the substrate 10 to form electrically conductive substances 3a, and only resin 2b (which becomes a cured resin 2a) remains outside the regions between opposing electrode pads 21 and lands 11.

To better illustrate the differences between the arrangement shown in Figure 7(e) of Segawa and the arrangement shown in Figures 12(a) and 12(b) of the present application, marked-up copies of Figure 6 of Segawa and of Figures 12(a) and 12(b) of the present application are shown on the following pages. Figure 6 of Segawa has been used instead of Figure 7(e) because it shows the same state as in Figure 7(e) but is much clearer than Figure 7(e).

【図6】



Regions between opposing electrodes

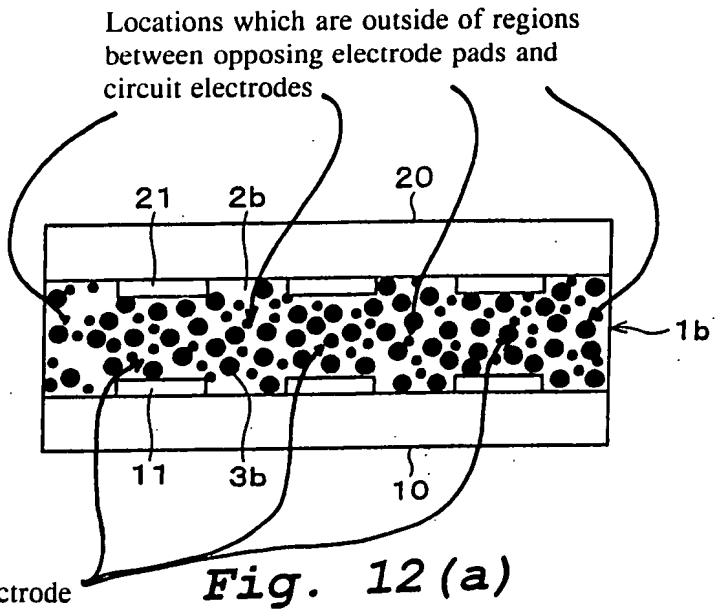


Fig. 12(a)

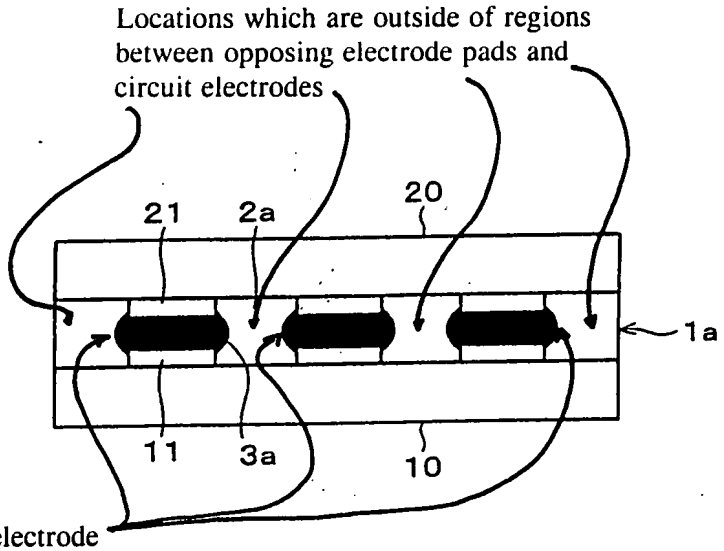


Fig. 12(b)

In the cross section of Figure 6 of Segawa, there are two regions between opposing pairs of electrodes 24a, 24b, etc. and 22a, 22b, etc., corresponding to the two pairs of electrodes. Each of these two regions is shown as having three electrically conductive particles sandwiched between opposing electrodes. In the same cross section, there are three "locations" lying outside of the regions between opposing pairs of electrodes: a location on the far right side of the figure, a location on the far left side of the figure, and a location between the two above-mentioned regions. The term "location" has been used here to avoid confusion with the "regions" between opposing pairs of electrodes, but a "location" could also be described as an area or a region, just not a region between opposing pairs of electrodes. Each of these "locations" in Figure 6 still has electrically conductive particles dispersed in it, and the number of electrically conductive particles in these locations exceeds the number of electrically conductive particles in the regions between opposing electrodes. As such, the method used to form the arrangement of Figure 6 (and Figure 7(e)) of Segawa does not include heating in which substantially all of the electrically conductive particles in a resin composition collect in regions between opposing electrode pads and circuit electrodes, as set forth in claim 13.

In the cross section of Figure 12(b) of the present application, there are three regions between opposing pairs of electrode pads 21 and circuit electrodes 11 (each region

corresponding to one of the pairs), and there are four "locations" lying outside of these three regions, i.e., two locations situated between adjoining regions, another location on the far right side of the arrangement, and another location on the far left side of the arrangement. All of the electrically conductive particles which were initially dispersed throughout the entire space between the semiconductor chip 20 and the substrate 10 have collected in the regions between the opposing electrode pads 21 and circuit electrodes 11, leaving only the resin outside of these three regions.

The method described by claim 13 provides a great improvement with respect to efficiency of operation as well as with respect to the properties of the resulting soldered connections over conventional methods of mounting IC chips, such as the method disclosed by Segawa. As mentioned above with respect to claims 8 and 11, in the method of Segawa, only a small number of the electrically conductive particles present in an anisotropic electrically conductive material are available for forming an electrical connection between an IC chip and a substrate, these being the electrically conductive particles which are capable of being trapped between opposing electrodes when the IC chip is forced against the substrate. As can be seen from above-described Figures 6 and 7(e), in the method of Segawa, a good portion if not most of the electrically conductive particles in the anisotropic electrically conductive material remain outside of the spaces between opposing electrodes, where

they serve no useful function. The presence of these particles in these areas reduces the electrical insulating ability of the resin which fills these areas, and since they have no utility in these areas, their presence represents economic waste. Because an electrical connection is created by just the small number of electrically conductive particles which are sandwiched between the IC chip and the substrate, the height of the solder joint which they formed is very small. Moreover, the electrically conductive particles, even when they melt, generally cannot cover the entire surface area of the opposing electrodes of the IC chip and the substrate, so the resulting soldered connections between the IC chip and the substrate have a high electrical resistance.

In contrast, according to the method set forth in claim 13, because substantially all of the electrically conductive particles in a resin composition collect in regions between opposing electrode pads and circuit electrodes, all of the electrically conductive particles in the resin composition can be put to effective use in forming an electrically conducting joint rather between the opposing electrode pads and circuit electrodes instead of being left dispersed in the resin and serving no useful function. Since the resin remaining outside the regions between opposing electrode pads and circuit electrodes is essentially devoid of the electrically conductive particles which have collected between the opposing electrode pads and circuit electrodes, the resin has better electrical insulating properties than the resin in similar locations in Figures 6 and 7(e) of

Segawa which has electrically conductive particles dispersed throughout it. Furthermore, since the joints between opposing electrode pads and circuit electrodes are formed by electrically conductive particles which have collected from throughout the space between the semiconductor chip and the circuit substrate, a large number of electrically conductive particles are available for forming the joints, and this enables the joints to have a large height as well as a large area of contact with the opposing electrode pads and circuit electrodes, which provides the joints with a reduced electrical resistance.

On page 6 of the Official Action, claim 9 was rejected under 35 USC 103(a) as unpatentable over Segawa in view of Ouchi et al (JP 2002-343829, referred to below as Ouchi). This rejection is respectfully traversed.

As discussed above, Segawa discloses a manufacturing method in which an IC chip is joined to a wiring board by an anisotropic electrically conductive material containing electrically conductive particles. Ouchi teaches a method of manufacturing a semiconductor device in which a semiconductor device 1 having bumps 2 formed on pads is connected to the pads 4 of a wiring board 3 by a thermosetting resin 6 applied atop the wiring board 3. The thermosetting resin 6 may contain a component with a fluxing action. According to the Official Action, it would have been obvious to have modified Segawa to employ an anisotropic electrically conductive material having reducing properties as

taught by Ouchi.

Claim 9 depends from claim 8, which as stated above describes a method of interconnecting terminals including heating a resin disposed between terminals with opposing terminals separated from each other by a space large enough to enable the particles to move inside the space. As discussed above with respect to claim 8, Segawa does not disclose or suggest such a method, since in Segawa, electrically conductive particles between electrodes are immobilized during heating. Ouchi, which was relied upon as teaching the use of a thermosetting resin having a fluxing action, discloses nothing about the use of a resin containing electrically conductive particles. Therefore, even if Segawa were combined with Ouchi in the manner proposed by the Official Action, the combined references would not result in a method including performing heating with opposing terminals separated from each other by a space large enough to enable the particles to move inside the space. As such, the combined references would not result in a method including all the steps set forth in claim 8 and included in claim 9 by its dependence from claim 8 and so cannot render claim 9 obvious. Claim 9 is thus allowable.

On page 8 of the Official Action, claims 14 and 15 were rejected under 35 U.S.C. 103(a) as unpatentable over Segawa. This rejection is respectfully traversed.

Claims 14 and 15 are allowable firstly by their dependence from claims 11 and 8, respectively, and are further allowable in their own right. Each of these claims includes a step of performing heating with opposing members being joined (opposing electrode pads and circuit electrodes in the case of claim 14, and opposing terminals in the case of claim 15) separated from each other by a distance which is at least a multiple of the diameter of the electrically conductive particles in an anisotropic electrically conductive resin composition. Segawa does not disclose or suggest such a step. As discussed above with respect to claims 8 and 11, in Segawa, during a heating step, the electrically conductive particles 6a, 6b, 26a, 26b, etc. in an anisotropic electrically conductive material 7, 27 are tightly compressed between the connecting electrodes of a bare chip IC and the electrodes of a wiring board or between solder bumps formed on a bare chip IC and the electrodes of a wiring board. There is no disclosure in Segawa concerning the number of electrically conductive particles which are sandwiched between the solder bumps and the electrodes of the wiring board with respect to the first embodiment of Figure 3, but with respect to the second embodiment of Segawa, Figures 6 and 7(e) clearly show a single layer of electrically conductive particles immobilized between opposing electrodes of a bare chip IC 24 and a wiring board 21. Nowhere in Segawa is there any disclosure or suggestion of opposing terminals or electrodes being spaced from each other by a distance which is at least a multiple of the diameter of the electrically conductive particles. The Official

Action does not provide any teachings that make up for the deficiencies of Segawa and would lead a person skilled in the art to modify the disclosure of Segawa. The Official Action states that "the claim range is considered to be an obvious matter of finding an optimum workable range for some chosen design requirement", by which the Official Action appears to mean that the spacing between opposing terminals or electrodes in the methods recited in claims 14 and 15 is merely a matter of choice. However, no such choice is offered by Segawa. The sole option presented by Segawa is for opposing electrodes of a bare chip IC and a wiring board to be spaced from each other such that a single layer of electrically conductive particles is gripped between the opposing electrodes. As such, a person skilled in the art could not receive any motivation from Segawa to modify it to employ a spacing different from the only spacing that Segawa teaches as being practicable. Accordingly, the grounds of rejection of claims 14 and 15 do not set forth a *prima facie* case of obviousness, and claims 14 and 15 are allowable.

In light of the foregoing remarks, it is believed that the present application is in condition for allowance. The proposed amendments to claims 8 and 11 are directly solely to correct typographical errors and do not affect the scope of the claims or raise new issues. Accordingly, entry of the proposed amendments is appropriate.

Favorable consideration is respectfully requested.

Respectfully submitted,

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Attachments:

Attachment A: partial translation of JP 2002-26070 (Segawa)
Attachment B: "CSP/MCM Mounting Technology", pages 182 - 185
Attachment C: "ThreeBond Technical News" (July, 1996)